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EXAMINER	
DANIELS, ANTHONY J	
ART UNIT	**PAPER NUMBER**
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,366	UYA, SHINJI	
	Examiner	Art Unit	
	Anthony J. Daniels	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/26/02

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,6-8 and 11-18 is/are rejected.

7)☒ Claim(s) 4,5,9 and 10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 February 2002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Thin-out Drive Method for CCD image sensor."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3,6-8,11,13,15,17 are rejected under 35 U.S.C. 102(b) as being anticipated by Udagawa et al. (US # 5,880,781).

As to claim **1**, Udagawa et al. teaches a solid-state image pickup device, (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*) comprising: a semiconductor substrate (*The semiconductor substrate is an inherent part of a CCD.*) having a two-dimensional plane on a surface thereof (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*); photoelectric converter elements arranged in a matrix configuration having rows and columns formed in said two-dimensional plane (see Figure 1; Col. 4, Lines 35,36); one vertical charge transfer channel region formed in said semiconductor substrate for each of the columns of said photoelectric converter elements, adjacent to said each column (see Figure 2B; Col. 4, Lines 36,37, "...VCCD."); two charge transfer electrodes so disposed over said vertical charge transfer channel regions for each of the rows of said photoelectric converter elements as to intersect said vertical charge transfer channel regions (see Figure 2A, V1, V2; *{The gates V1 and V2 are used for the single row of pixels starting with C1; pulses are applied to the row starting C1, so it is inherent that there is some sort of electrical connection disposed over the charge transfer region.}*); an array of color filters each of which is formed for each of said photoelectric converter elements over said each photoelectric converter element (Figure 2A, rows starting C1 and M1; Col. 4, Lines 30-34), said array including color layouts each of which includes n rows of said color filters (see Figure 1, Figure 2A; *{Applicant does not define n in the specification*

nor in the claims; therefore, examiner interprets n as being any number unless explicitly defined in the claims. In this particular case, n is 2.}); and a drive circuit for conducting a readout operation (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) in which (m*n) rows of photoelectric converter elements are classified as one set (see Figure 2A; *{Applicant does not define n nor m in the specification nor in the claims; therefore examiner interprets n and m as being any number. In this particular case, n is two and m is four; thus, the set consist of eight rows (rows C1 – M3).}*, a plurality of units of photoelectric converter element rows (see Figure 2A, *{The rows starting with C1 and M1 together are considered a unit, and C3 and G3 together are considered a unit.}*) which are symmetrically distributed (see Figure 2A; *{If the axis of symmetry were drawn between V2 and V3 then this would be a symmetric distribution of this unit (Applicant does not define an axis of symmetry.).}*) are respectively selected from said sets of photoelectric converter element rows (see Figure 2B, C1 and M1 are selectively read out), and electric charge is read from said plural units of photoelectric converter element rows to be fed to said vertical charge transfer channel regions (see Figure 2B, Figure 2C), said readout operation comprising: a first readout operation for reading electric charge from a first group of photoelectric converter element rows which have an asymmetric distribution (see Figure 2B; *{The first **group** of rows are considered the rows starting with M1 and C3; furthermore, if the axis of symmetry were drawn between G2 and C3, the distribution of this group would be considered asymmetric (Applicant does not define an axis of symmetry.).}*), into said vertical charge transfer channel regions (see Figure 2B); a j-row transfer operation for transferring the electric charge for j rows after said first readout operation (see Figure 2D; *{The downward transfer of the addition of C and M is considered by the examiner to be the j-row transfer*

operation, since applicant gives no clear definition of what the j-row transfer is.}), and a second readout operation for reading electric charge from a second group of photoelectric converter element rows which have an asymmetric distribution at positions to which the electric charge is transferred by said j-row transfer operation, into said vertical charge transfer channel regions (see Figure 2B; *{The second* ***group*** *of rows are considered the rows starting with C1 and G3; furthermore, if the axis of symmetry were drawn between G2 and C3, the distribution of this group would be considered asymmetric in the vertical direction which is the position to which electric charge is transferred by said j-row transfer operation.}*; ***{Applicant should note that the examiner does not interpret first and second as chronologically defining adjectives for the readout operation; that is to say the first and second readout operations transpire simultaneously, and the j-row operation occurs after the first readout operation and the second readout operation.}***), and for adding the electric charges to each other in said vertical charge transfer channel regions (see Figure 2D), said first and second readout operations reading electric charge from two rows included in one unit of photoelectric converter element rows (see Figure 2B; *{C1 and M1 are readout from the first and second operations, respectively, and they are from two rows of the same unit.}*).

As to claim **2**, Udagawa et al. teaches the solid-state image pickup device according to claim 1, wherein: said n is two; said m is four (see Figure 2A; *{If n is two and m is four, the set would consist of eight rows (m*n)(C1-M3), which is shown in Figure 2A}*); and said selected units selected by said readout operation are two units per said set (see Figure 2B, *{The two selected units of C1,M1 (UNIT 1) and C3,G3 (UNIT 2) are the only units readout in the set of eight in Figure 2B.}*).

As to claim **3**, Udagawa et al. teaches the solid-state image pickup device according to claim 2, wherein: said selected units are obtained from every second unit (see Figure 2B; *{Examiner is interpreting a unit as two rows; consequently, Figure 2B would show that a unit is selected every second unit in Figure 2B.}*); said first readout operation is conducted for a second row of a first selected first unit (see Figure 2B; the row starting with M1) and for a first row of a second selected unit (see Figure 2B; the row starting with C3); and said second readout operation is conducted for a first row of said first selected first unit (see Figure 2B; the row starting with C1) and for a second row of said second selected unit (see Figure 2B; the row starting with G3).

As to claims **6-8**, claims 6-8 are method claims corresponding to the apparatus claims 1-3, respectively. Therefore, claims 6-8 are analyzed and rejected as previously discussed with respect to the apparatus claims 1-3, respectively.

As to claim **11**, Udagawa et al. teaches a solid-state image pickup device (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*), comprising: a semiconductor substrate (*The semiconductor substrate is an inherent part of a CCD.*) having a two-dimensional plane on a surface thereof (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*); a plurality of photoelectric converter elements arranged in the two-dimensional plane in a matrix configuration having rows and columns (see Figure 1; Col. 4, Lines 35,36); an array of color filters including one color layout of two rows as one unit (see Figure 1; rows starting C Y C and M G M are a unit, said unit being repeatedly arranged in said array in a column direction (see Figure 1, Col. 3, Lines 14-17) in which one color filter thereof is formed over each of said photoelectric converter elements (see Figure 1; Col. 4, Lines 30-34), said two rows including a row of a first color layout

of color filters arranged in a row direction (see Figure 1; row starting C Y C) and a row of a second color layout of color filters arranged in a row direction (see Figure 10, row starting M G M), said second color layout being different from said first color layout (see Figure 1; *{C Y C is different from M G M.}*); one vertical charge transfer channel region formed in said semiconductor substrate for each of the columns of said photoelectric converter elements, adjacent to said each column (see Figure 2B; Col. 4, Lines 36,37, "...VCCD."); a plurality of vertical charge transfer electrodes in which two vertical charge transfer electrodes are disposed over said vertical charge transfer channel regions for each of the rows of said photoelectric converter elements (see Figure 2A, V1, V2; *{The gates V1 and V2 are used for the single row of pixels starting with C1; pulses are applied to the row starting C1, so it is inherent that there is some sort of electrical connection disposed over the charge transfer region.}.}*); and a drive circuit capable of applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes corresponding to said photoelectric converter element row having said first color layout in a first photoelectric converter element row pair (see Figure 2A; *{V1-V4 are applied to rows starting C1 and M1.}*) of two photoelectric converter element rows adjacent to each other in a column direction (see Figure 2A; *{C1 and M1 are adjacent to each other in the column direction.}*) and to said vertical charge transfer electrodes corresponding to said photoelectric converter element row having said second color layout in a second photoelectric converter element row pair (see Figure 2A; *{V1-V4 are applied to rows starting C3 and G3.}*) of two photoelectric converter element rows adjacent to each other in a column direction (see Figure 2A; *{C3 and G3 are adjacent to each other in the column direction.}*), said second photoelectric converter element row pair being at a position apart from

said first photoelectric converter element row pair by two photoelectric converter element rows in the column direction (see Figure 2A; *{The **two** rows starting Y2 and G2 separate the first row pair (C1 and M1) and the second row pair (C3 and G3)}*).

As to claim **13**, Udagawa et al. teaches a solid-state image pickup device (see Figure 1, Figure 2A; Col. 4, Lines 30-34*; {The color layout of Figure 1 is used on the CCD of Figure 2A.}*), comprising: a semiconductor substrate (*The semiconductor substrate is an inherent part of a CCD.*) having a two-dimensional plane on a surface thereof (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*); a plurality of photoelectric converter elements arranged in the two-dimensional plane in a matrix configuration having rows and columns (see Figure 1; Col. 4, Lines 35,36); an array of color filters including one color layout of n rows as one unit (see Figure 1; *{Applicant defines a unit as two rows; therefore, n is 2.}*), said unit being repeatedly arranged in a row direction in said array (see Figure 1; rows starting C Y C and M G M as a unit), said n rows ranging from a first row to an n-th row respectively having mutually different color layouts in the row direction (see Figure 1, rows starting C Y C and M G M have mutually different color layouts) in which one color filter of said array is formed over each of said photoelectric converter elements (see Figure 1; Col. 4, Lines 30-34); one vertical charge transfer channel region formed in said semiconductor substrate for each of the columns of said photoelectric converter elements, adjacent to said each column (see Figure 2B; Col. 4, Lines 36,37, "...VCCD."); a plurality of vertical charge transfer electrodes in which two vertical charge transfer electrodes are disposed over said vertical charge transfer channel regions for each of the rows of said photoelectric converter elements (see Figure 2A, V1,V2,V3,V4, etc.; *{The gates V1 and V2 are used for the single row of pixels starting with*

C1; and as can be seen from Figure 2A, the two electrodes per row continues down the set.}); and a drive circuit capable of independently applying readout pulse voltages (see Figure 1, Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes (see Figure 2A, V3,V4) included in said photoelectric converter element rows having mutually different color layouts between said photoelectric converter element row units (see Figure 2A; rows starting Y2 and G2 have different color layouts and are between the aforementioned units), said photoelectric converter element rows being included in a set of n rows (see Figure 2A; *{Examiner assumes a set of 2 rows.}*) including a first photoelectric converter element row having said first color layout (see Figure 2A, row starting C1), said first row being selected from said first photoelectric converter element row unit (see Figure 2A, unit consists of rows starting C1 and M1) including n rows succeeding one after another in a column direction (see Figure 2A, rows of 2 succeed one after another in Figure 2A) and second to n-th photoelectric converter element rows (see Figure 2A, row starting G3) sequentially formed at positions beginning at a position apart from said first photoelectric converter element row unit by (2 X n) photoelectric converter element rows in the column direction (see Figure 2A, row starting G3 is four rows (2 X (n=2)) apart from row starting C1).

As to claim **15**, Udagawa et al. teaches a method of controlling a solid-state image pickup device (see Figure 1, Figure 2A; Col. 4, Lines 30-34*; {The color layout of Figure 1 is used on the CCD of Figure 2A.}*), comprising a semiconductor substrate (*The semiconductor substrate is an inherent part of a CCD.*) having a two-dimensional plane on a surface thereof (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*); a plurality of photoelectric converter elements arranged in the two-dimensional plane in a

matrix configuration having rows and columns (see Figure 1; Col. 4, Lines 35,36); an array of color filters including one color layout of two rows as one unit (see Figure 1; rows starting C Y C and M G M are one unit), said unit being repeatedly arranged in said array in a column direction (see Figure 1; Col. 3, lines 14-17), said two rows including a row of a first color layout of color filters arranged in a row direction in which one color filter thereof is formed over each of said photoelectric converter elements (see Figure 1, row starting C Y C; Col. 4, Lines 30-34) and a row of a second color layout of color filters arranged in a row direction, said second color layout being different from said first color layout (see Figure 1, row starting M G M); one vertical charge transfer channel region formed in said semiconductor substrate for each of the columns of said photoelectric converter elements, adjacent to said each column (see Figure 2B; Col. 4, Lines 36,37, "...VCCD."); a plurality of vertical charge transfer electrodes in which two vertical charge transfer electrodes are disposed over said vertical charge transfer channel regions for each of the rows of said photoelectric converter elements (see Figure 2A, V1, V2,V3,V4, etc.; *{The gates V1 and V2 are used for the single row of pixels starting with C1; and as can be seen from Figure 2A, there are two electrodes for each row continuing down the set.}*); and a drive circuit capable of applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes corresponding to said photoelectric converter element row having said first color layout in a first photoelectric converter element row pair of two photoelectric converter element rows (see Figure 2A; V3 and V4 belonging to the row starting M1) succeeding one after another in a column direction (see Figure 1; Col. 3, Lines 14-17) and to said vertical charge transfer electrodes corresponding to said photoelectric converter element row (see Figure 2A; V1 and V2 belonging to C3) having said second color

layout in a second photoelectric converter element row pair (see Figure 2A, C3 and G3 are a row pair and have a different second color layout) of two photoelectric converter element rows contiguous to each other in a column direction (see Figure 2A), said second photoelectric converter element row pair being at a position apart from said first photoelectric converter element row pair by two photoelectric converter element rows in the column direction (see Figure 2A; the ***two*** rows starting Y2 and G2 separate the aforementioned row pairs), said method comprising the steps of: classifying said vertical charge transfer electrodes into sets each of which includes 16 vertical charge transfer electrodes as one set (see Figure 2A; *{There are two sets of 8 pulses (V1-V8).}*, said 16 vertical charge transfer electrodes ranging from a first vertical charge transfer electrode to a 16th vertical charge transfer electrode succeeding one after another (see Figure 2A), and applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes belonging to said photoelectric converter element row having said first color layout of said first photoelectric converter element row pair (see Figure 2A, V1,V2 belonging to row starting C1) including two rows adjacent to each other in the column direction (see Figure 2A, row starting C1 and M1), said first row pair being selected from each said set (see Figure 2B, rows starting C1 and M1; *{Udagawa et al. is also a thin-out readout method (see Abstract, Lines 5,6.}*) and to said vertical charge transfer electrodes belonging to said photoelectric converter element row having said second color layout different from said first color layout of said second photoelectric converter element row pair (see Figure 2A, V1,V2 belonging to C3; G3 and C3 row pair is different from C1 and M1) including two rows adjacent to each other in the column direction (see Figure 2A, rows starting C3 and G3) said row pair being formed in positions beginning at a position apart from said first photoelectric

converter element row pair by four photoelectric converter element rows in the column direction (see Figure 2A ; *{The row starting C1 and the row starting C3 are 4 rows apart, each from different row pairs.}*) b) transferring the signal charge read out by said step a) through said vertical charge transfer channel regions for four photoelectric converter element rows in column direction (see Figure 2D; *{The j-row transfer operation transfers the addition of charges to a HCCD, which would have to be at least four photoelectric converter element rows apart from the row starting C1 according to Figure 2D.}*); c) applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes belonging to said photoelectric converter element rows of said first and second photoelectric converter element row pairs (see Figure 2B, V1-V4 of rows starting C1 and M1 and V1-V4 of rows starting C3 and G3), said photoelectric converter element rows being not used to read the electric charge therefrom in said step a) (see Figure 2C, rows starting Y2,G2 and Y3,M3); and d) transferring the electric charge read out in said step c) and the electric charge read out in said step a) in said vertical charge transfer channel regions (see Figure 2C; Col. 4, Lines 36,37, "...VCCD.").

As to claim **17**, Udagawa et al. teaches a method of controlling a solid-state image pickup device (see Figure 1, Figure 2A; Col. 4, Lines 30-34*; {The color layout of Figure 1 is used on the CCD of Figure 2A.}*), comprising a semiconductor substrate (*The semiconductor substrate is an inherent part of a CCD.*) having a two-dimensional plane on a surface thereof (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*); a plurality of photoelectric converter elements arranged in the two-dimensional plane in a matrix configuration having rows and columns (see Figure 1; Col. 4, Lines 35,36); an array of color filters including one color layout of n rows as one unit see Figure 1; *{Applicant defines a*

unit as two rows; therefore, n is 2.}), said unit being repeatedly arranged in a row direction in said array (see Figure 1), said n rows ranging from a first row to an n-th row respectively having mutually different color layouts in the row direction (see Figure 1, row starting C Y C) in which one color filter of said array is formed over each of said photoelectric converter elements (see Col. 4, Lines 30-34); one vertical charge transfer channel region formed in said semiconductor substrate for each of the columns of said photoelectric converter elements, adjacent to said each column (see Figure 2B; Col. 4, Lines 36,37, "...VCCD."); a plurality of vertical charge transfer electrodes in which two vertical charge transfer electrodes are disposed over said vertical charge transfer channel regions for each of the rows of said photoelectric converter elements (see Figure 2A, V1, V2; *{The gates V1 and V2 are used for the single row of pixels starting with C1; two for each can be seen in Figure 2A.}*); a drive circuit capable of independently applying readout pulse voltages to said vertical charge transfer electrodes included in said photoelectric converter element rows (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) having mutually different color layouts in said photoelectric converter element row units (see Figure 1, Figure 2A), said photoelectric converter element rows being included in a set of n rows (see Figure 2A; *{Examiner assumes a set of 2 rows.}*) including a first photoelectric converter element row having said first color layout (see Figure 2A, row starting C1), said first row being selected from said first photoelectric converter element row unit (see Figure 2A, unit consists of rows starting C1 and M1) including n rows succeeding one after another in a column direction (see Figure 2A, rows of 2 succeed one after another in Figure 2A) and second to n-th photoelectric converter element rows (see Figure 2A, row starting G3) sequentially formed at positions beginning at a position apart from said first photoelectric converter element row unit by (2 X n) photoelectric

converter element rows in the column direction (see Figure 2A, row starting G3 is four rows (2 X (n=2)) apart from row starting C1), said method comprising the steps of: a) classifying said vertical charge transfer electrodes into sets each of which includes (4 X n) vertical charge transfer electrodes as one set (see Figure 2A; *{A set in this case is eight with n equal to 2.}*), and independently applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes (see Figure 2A, V1,V2) included in said photoelectric converter element rows having mutually different color layouts in said photoelectric converter element row units (see Figure 2A, unit C1 and M1 and unit C3 and G3), said photoelectric converter element rows being included in a set of n rows including a first photoelectric converter element row having said first color layout (see Figure 1, row starting C Y C), and second to n-th photoelectric converter element rows at positions beginning at a position apart from said first photoelectric converter element row unit by (2 X n) photoelectric converter element rows in the column direction and at a same pitch (see Figure 1, row starting G M G); b) transferring signal charge read out by said step a) through said vertical charge transfer channel regions (see Figure 2C; Col. 4, Lines 36,37, "...VCCD.") for (2 X n) photoelectric converter element rows in column direction (*In order to get to the HCCD, it is inherent that the rows be transferred for 4 rows (2 X (n=2))*).; and conducting a readout operation and a transfer operation (see Figure 2C and Figure 2D) for said vertical charge transfer electrodes belonging to said photoelectric converter element rows of said photoelectric converter element row unit (see Figure 2A, rows starting C1 and M1 as one unit) including said first to n-th photoelectric converter element row pairs (see Figure 2A, rows starting C1 and M1 as a row pair), said

photoelectric converter element rows being not used to read the electric charge therefrom in said step a) (see Figure 2C; rows starting Y2 and G2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12,14,16,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Udagawa et al. (see Patent Number above) in view of Tanaka et al. (US 6,559,889).

As to claim **12**, Udagawa et al. teaches the solid-state image pickup device according to claim 11, the claim differs from Udagawa et al. in that it further requires a variable barrier formed in said semiconductor substrate below said photoelectric converter elements, said variable barrier being capable of modulating an amount of electric charge accumulable in each of said photoelectric converter elements.

In the same field of endeavor, Tanaka et al. teaches that the amount of signal charge accumulated in each sensor of a CCD array is determined by a potential barrier height (*Changing the barrier height changes or modulates the amount of charge received in the photosensors.*) of an overflow barrier that is formed in a p-type well region (see Figure 5, p-type well region "31"; see Col. 4, Lines 52-61) formed below the sensor section (see Figure 5, *{The only thing below the p-type region "31" is the n-type substrate; thus, the p-type well region has to be formed below the photosensors.}*). In light of the teaching of Tanaka et al., it would have been obvious to

one of ordinary skill in the art at the time the invention was made to modify the semiconductor substrate of Udagawa et al. to include a p-type well region that determines the amount of charge accumulable in each photosensor, because one of ordinary skill in the art would recognize that this would allow the saturation signal charge amount to increase or decrease in anticipation of reduction, thereby preventing such characteristics as S/N ratio and dynamic from being deteriorated due to the reduction of saturation signal charge amount (see Tanaka et al., Col. 7, Lines 51-62).

As to claim **14**, Udagawa et al., as modified by Tanaka et al., teaches the solid-state image pickup device according to claim 13, further comprising a variable barrier formed in said semiconductor substrate below said photoelectric converter elements (see Tanaka et al., Figure 5, p-type well region "31"; *{The only thing below the p-type region "31" is the n-type substrate; thus, the p-type well region has to be formed below the photosensors.}*) said variable barrier being capable of modulating an amount of electric charge accumulable in each of said photoelectric converter elements to n times an original amount thereof (see Tanaka et al., Col. 7, Lines 51-62; *{By lowering Vsub, the amount signal charge acumulable can be increased. Since n is not defined by applicant, examiner chooses n to be a value to which allows Tanaka et al. to meet the limitations of this claim.}*).

As to claim **16**, Udagawa et al., as modified by Tanaka et al., teaches the method of controlling a solid-state image pickup device according to claim 15,wherein said device further comprises a variable barrier formed in said semiconductor substrate, said variable barrier being capable of modulating an amount of electric charge accumulable in each of said photoelectric converter elements (see Tanaka et al., Figure 5, p-type well region "31"; Col. 4, Lines 52-61)

said method further comprising the step of x) modulating by said variable barrier an amount of electric charge accumulable in each of said photoelectric converter elements to one half of an original amount thereof before said step a) (see Col. 7, Lines 51-62; *{By increasing Vsub, the amount signal charge acumulable can be decreased. It is inherent in this system of Tanaka et al. that Vsub could be set to a value which allows the amount of charge to be decreased by one-half.}*).

As to claim **18**, Udagawa et al., as modified by Tanaka et al., teaches the method of controlling a solid-state image pickup device according to claim 17, wherein said device further comprises a variable barrier formed in said semiconductor substrate, said variable barrier being capable of modulating an amount of electric charge accumulable in each of said photoelectric converter elements (see Tanaka et al., Figure 5, p-type well region "31"; Col. 4, Lines 52-61), said method further comprising the step of x) controlling said variable barrier to modulate an amount of electric charge accumulable in each of said photoelectric converter elements to l/n of an original amount thereof before said step a) (see Tanaka et al., Col. 7, Lines 51-62; *{By lowering Vsub, the amount signal charge acumulable can be decreased. Since n is not defined by applicant, examiner chooses n to be a value to which allows Tanaka et al. to meet the limitations of this claim.}*).

Allowable Subject Matter

6. Claims 4,5,9,10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: As to claim **4,9**, the prior art does not teach or fairly suggest a solid-state image pickup device wherein set of pixels in which 18 pixel rows are classified as a set. As to claim **5,10**, claims 5,10 are allowable as being dependent upon the dependent claims 4,9, respectively.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Thai Tran can be reached on (571) 272-7382. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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AD
2/8/2005

NGOC-YEN VU
PRIMARY EXAMINER